REMARKS

In the Office Action, the Examiner indicated that claims 1-13 are pending in the application and that all of the pending claims are rejected.

Rejection Under 35 U.S.C. §103

To support a rejection under 35 U.S.C. §103, a reason, suggestion, or motivation to lead an inventor to combine two or more references must be found. *Pro-Mold and Tool Co. v. Great Lakes Plastics Inc.*, 37 U.S.P.Q.2d 1627, 1629 (Fed.Cir. 1996). The Examiner has not met his burden in establishing a reason, suggestion, or motivation for combining the cited references, as discussed below.

The Present Invention

The present invention relates to an interface utilizing existing clock signals from a driver circuit, such as a DSP, to charge capacitors that are normally used for capacitive coupling of digital data across a high voltage isolation barrier. Using relatively small capacitors (e.g., capacitors in the range between 10 pF and 500 pF, and preferably at 100 pF) a charge pump is formed to generate power to the interface at all times. Thus, the interface always has a steady source of power available for use, including during the on-hook state, for powering circuitry that can detect, modulate, and transmit on-hook signals across the capacitive interface.

The claimed invention includes circuitry that doubles the voltage of the clock signal coming from the DSP, thereby obtaining more power for use by a data access arrangement (DAA) coupled to the interface and, therefore to the DSP. Further, the interface circuit is a fully differential circuit, thereby eliminating the need to keep the impedance across the

capacitive coupling low, as is required when using a pseudo-differential interface circuit.

Hein et al., U.S. Patent No. US 6,198,816 B1

U.S. Patent No. 6,198,816 teaches a communication system utilizing a capacitive isolation barrier to linearly attenuate the tip/ring signal voltage levels from the high phone line levels to levels within integrated circuit technology limitations. The Hein isolation circuit illustrated, for example, in Fig. 13A and Fig. 13B, is a pseudo-differential circuit. The capacitive isolation barrier of Hein requires very large capacitors, e.g., at least 10,000 pF. With the large capacitances required by Hein, the impedance is low with respect to the signals across the capacitance; thus, is done by Hein to avoid the extensive filtering that must be utilized to filter out existing common mode signals and also common mode signals generated by the interface itself if lower capacitances were used in connection with the pseudo-differential circuit.

Hershbarger et al., U.S. Patent No. 5,664,984

Hershbarger et al. teach a method and apparatus for communicating a modulated signal across an isolation barrier using capacitors, similar to the capacitive isolation barrier of Hein et al. Like Hein, Hershbarger utilizes a pseudo-differential circuit which is thus very sensitive to impedance, thereby requiring that the capacitive coupling have a high value, e.g., 10,000 pF. Hershbarger is relied upon by the Examiner for its teaching of the use of a DSP with a charge pump for high voltage isolation for a DAA.

Kan et al., U.S. Patent No. 6,020,773

Kan et al. teaches a clock signal generator for generating a plurality of clock signals with different phases.

The Claimed Invention Is Not Taught or Suggested by Hein, Hershbarger or Kan, Either Alone or in Combination

As noted above, to support a rejection under 35 U.S.C. §103, the cited references must suggest a reason, suggestion, or motivation to lead an inventor to combine two or more references must be found. None of the references cited by the Examiner teach or suggest a driver circuit, such as a charge pump, which doubles the voltage of a clock signal provided by the driver circuit to thus increase the voltage available for use by a DAA. In addition, none of Hein, Hershbarger, or Kan teach or suggest the use of a fully differential signal processing circuit and thus require very large value capacitors and/or filtering elements if the size of the capacitors are reduced.

The claims of the present invention, as amended, positively recite these novel and distinguishing features (claim 1, "a charge pump ... doubling the voltage of said clock signal"; claim 8, "a charge pump ... doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power."; claim 14, "An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit"; claim 15, "An interface circuit as set forth in claim 2 wherein said first capacitive element has: a maximum capacitance of 500 pF; and a minimum capacitance of 10 pF."). Since none of these elements are taught or suggested by Hein, Hershbarger or Kan, it is submitted that the claims, as amended, patentably define over the cited references.

Conclusion

The claims, as amended, patentably define over the prior art cited by the Examiner in rejecting the claims. Accordingly, reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 1 has been amended as follows:

1. (Amended) An interface circuit, comprising:

a digital signal processor (DSP) generating a clock signal having a voltage;

a data access arrangement (DAA); and

a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said clock signal.

Claim 2 has been amended as follows:

2. (Amended) An interface circuit as set forth in claim 1, wherein said charge pump comprises:

a first capacitive element having an input side connected to said DSP and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said clock signal from said DSP and doubling the voltage of said clock signal before passing said clock signal to said DAA.

Claim 7 has been amended as follows:

7. (Amended) A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

inserting a charge pump between said DSP and said DAA;

generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump; and

doubling the voltage of said power signal and storing said generated power signal for use by said interface.

Claim 8 has been amended as follows:

8. (Amended) An interface circuit, comprising:

a driver circuit for developing a charge across capacitive elements of said interface circuit, said charge having a voltage;

a data access arrangement (DAA); and

a charge pump, coupled between said [DSP] DAA and said driver circuit, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power.

Claim 9 has been amended as follows:

9. (Amended) An interface circuit as set forth in claim 8, wherein said charge pump comprises:

a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said charge from said driver circuit and doubling the voltage of said charge before passing said charge to said DAA.

New Claims 14 to 19 have been added as follows:

--14. (New) An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit.

15. (New) An interface circuit as set forth in claim 2, wherein said first capacitive element has:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF.

16. (New) An interface circuit as set forth in claim 2, wherein the first capacitive element has a capacitance value of approximately 100 pF.

17. (New) An interface circuit as set forth in claim 8, wherein said interface circuit is a fully differential circuit.

18. (New) An interface circuit as set forth in claim 9, wherein said first capacitive element has:

a maximum capacitance of 500 pF; and

a minimum capacitance of 10 pF.

19. (New) An interface circuit as set forth in claim 9, wherein the first capacitive element has a capacitance value of approximately 100 pF.--